AMENDMENTS

In the Specification

Please add the following paragraph after line 8, page 6:

FIG. 10 is a cross-section of forming the CPU scheme under two layers of conductive ring.

Please amend the paragraph beginning on page 10, line 27 as follows:

FIG. 3A is a cross-section of another conductive ring underlying the conductive ring 26. Elements similar to those in FIG. 2A are omitted here. A second dielectric layer 36 underlying the first dielectric layer 24 is provided. A third conductive layer 38 is patterned as a ring and embedded in the second dielectric layer 36. A conductive plug 40 also is formed in the second dielectric layer 36 to electrically connect the conductive ring 26 to the ~~second~~ third conductive layer 38.

Please amend the paragraph beginning on page 11, line 6 as follows:

FIG. 3B is a cross-section of a conductive lattice underlying the conductive ring 26. Elements similar to those in FIG. 3A are omitted here. The third conductive layer 38 is modified to form a lattice, in which an array of dielectric islands 36a is provided and the dielectric islands 36a are spaced apart from each other by the third conductive layer 38. Alternately, the third conductive layer 38 is modified to form an array of independent plugs spaced apart from each other by the second dielectric layer 36.

Please amend the paragraph beginning on page 14, line 12 as follows:

In FIG. 7A, the conductive ring comprises two marking notches 46, and two dielectric markings 24b are correspondingly defined within the two marking notches 46, respectively. The two marking notches 46 are approximately aligned in a line to delineate the sensing region II from the bonding region I. Each of the two marking notches 46 is composed of a bottom side 46I and two lateral sides 46II and 46III. Preferably, a first-direction length L_1 from the lateral side ~~46II~~ 46III to the edge of the conductive ring 26 for defining the bonding region I is approximately 40 ~ 60 μm. Preferably, a first length S_1 of the dielectric marking 24b, parallel to the bottom side 46I, is approximately 1 ~ 3 μm. Preferably, a second length S_2 of the dielectric marking 24b, parallel to the lateral side 46II, is approximately 0.5 ~ 2 μm.

Please amend the paragraph beginning on page 14, line 26 as follows:

In FIG. 7B, the conductive pad 32 comprises two marking notches 48, and two passivation markings 30b are correspondingly defined within the two marking notches 48, respectively. The two marking notches 48 are approximately aligned in a line to delineate the sensing region II from the bonding region I. Each of the two marking notches 48 is composed of a bottom side 48I and two lateral sides 48II and 48III. Preferably, a first-direction length [L_1] L_2 from the lateral side ~~48II~~ 48III to the edge of the conductive pad 32 for defining the bonding region I is approximately 40 ~ 60 μm. Preferably, a first length S_1 of the passivation marking 30b, parallel to the bottom side 48I, is approximately 1 ~ 3 μm. Preferably, a second length S_2 of the passivation marking 30b, parallel to the lateral side 48II, is approximately 0.5 ~ 2 μm.